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EDS- 1547FF1C+ DVB-S Full NIM Tuner

SPECIFICATION

Taigo RF Technology (HK) Ltd Earda Technology Ltd.			
DSGD.	CHKD.	APPD.	PRODUCT：DVB-S Full NIM Tuner
			MODEL：EDS- 1547FF1C+
			DATE：2008.09.10

E-mail：earda@china.com

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[1]GENERAL SPECIFICATIONS

- Input frequency 950MHz —— 2150MHz
- Output frequency 950MHz —— 2150MHz
- Input signal level -65dBm —— -25dBm
- Input connector F-Connector
- Output connector F-Connector
- Input impedance 75Ω
- Output impedance 75Ω
- Channel selection system PLL synthesizer (Clock 4.0MHz I^2C bus interface)
- LINK IC STV0288（CLOCK：4MHz ， Address：D0（HEX））
- Operating voltage LNB power supply 25V DC, 400mA(MAX.)
  B2： +5V ± 0.25V
  B3： + 3.3V ± 0.165V
  VDD： + 2.5V ± 0.125V
- Temperature 0℃ ~ +60℃
  Storage:-20℃ ~ +70℃
- Humidity Operating: Less than 85%
  Storage: Less than 95%

KEY FEATURES

- DVB-S / DIRECTV™ full NIM tuner with autoscan feature
- Symbol rate 1 ~ 45Msps
- Fast channel acquisition
  - High speed scanning mode for blind symbol rate acquisition
  - Full satellite transponders scanning in seconds
- Up to 60 Msps operation
- DiSEqC™2.x
  - Receive and transmit for full control of LNB And switchers

MULTISTANDARD DECODING

- **DIRECTV™ system /DVB-S**
  - VITERBI soft decoder rate 1/2
  - Puncture rates are 1/2,2/3,3/4,5/6,6/7,7/8
  - Outer Reed-Solomon decoder as per DVB-S and DIRECTV™ system
  - Energy dispersal descrambler

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INTERFACES

- Data to transport decoder
  - DVB common interface compliant
  - 12-bit parallel and 5-bit serial data interface with Data on D0…D7 (packer error private line)
  - Transport bit rate automatic regulation with regard to transport clock
- I^2C serial bus interface
  - Fast I^2C up to 4 MbPs slave interface
  - 4 possible slave addresses
  - Up to 400 KbPs private repeater for tuner isolation
- DiSEqC™ 2.x
  - 22KHz to 100 KHz interface
- GPIOs and interruption line
  - lock indicators: AGC carrier, timing, VITERBI-decoder
- Monitoring through I^2C serial interface
  - C/N estimator-signal strength indicator
  - IQ constellation display
  - BER and PER estimator
  - Bit and packet error count

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[2]ELECTRICAL SPECIFICATION

Item	Condition		Specification			
			Min.	Typ.	Max.	Unit
RF input VSWR	950MHz —— 2150MHz			2.0	2.5	
RF output VSWR	950MHz —— 2150MHz			2.0	2.5	
RF output gain	950MHz —— 2150MHz		-2	0	+2	dB
Noise figure	950MHz —— 2150MHz Max gain			8	12	dB
Intermodulation rejection Desired signal Fo Undesired signal(2 signals) (Fo+29.5MHz,Fo+59MHz) or (Fo-29.5MHz,Fo-59MHz)	Input level -25dBm I/Q Output level 0.6Vp_p 1KΩ load		40	60		dB
Local oscillation signal Leak at input terminal	950MHz —— 2105MHz			-72	-68	dBm
Local oscillation signal Leak at output terminal	950MHz —— 2150MHz			-67	-63	dBm
Eb/No (BER=2×10^{-4} at Viterbi output）	4≦Fs≦35[Mbaud] （Fs: Symbol rate）	PC= 1/2		3.7	4.5	dB
		PC= 2/3		4.2	5.0	dB
		PC= 3/4		4.7	5.5	dB
		PC= 5/6		5.3	6.0	dB
		PC= 7/8		5.7	6.4	dB
Eb/No（Low rate） (BER=2×10^{-4} at Viterbi output）	1≦Fs<4[Mbaud] （Fs: Symbol rate）	PC= 1/2		4.8	5.5	dB
		PC= 2/3		5.0	6.0	dB
		PC= 3/4		5.5	6.5	dB
		PC= 5/6		6.2	7.0	dB
		PC= 7/8		6.8	7.4	dB
Eb/No（High rate） (BER=2×10^{-4} at Viterbi output）	35<Fs≦45[Mbaud] （Fs: Symbol rate）	PC= 1/2		4.4	5.4	dB
		PC= 2/3		5.1	6.1	dB
		PC= 3/4		6.0	7.0	dB
		PC= 5/6		6.9	7.9	dB
		PC= 7/8		7.5	8.5	dB
Current consumption	B2=5V			200	220	mA
	B3=3.3V			10	50	mA
	VDD=2.5V			250	350	mA

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[3]PLL FUNCTIONAL DESCRIPTION

I² C BUS DATA FORMATS

Table1：Write data format（MSB is transmitted first）Write address: C2(HEX), Read address: C3(HEX)

Sub address	B7	B6	B5	B4	B3	B2	B1	B0
01	OSCH	OCK1	OCK0	ODIV	OSM3	OSM2	OSM1	OSM0
02	N8	N7	N6	N5	N4	N3	N2	N1
03	N0	0	0	A4	A3	A2	A1	A0
04	0	0	0	0	0	1	0	0
05	0	0	0	0	G3	G2	G1	G0
06	0	0	0	F4	F3	F2	F1	F0
07	1	1	0	1	1	0	0	0
08	1	1	0	1	0	0	0	0
09	0	1	0	1	0	0	0	0
0A	1	1	1	0	1	0	1	1
0B	0	1	0	0	1	1	1	1

OSCH，OCK1-0，ODIV，OSM3-0（Reg01）：

LO. Frequency（MHz）	Data (HEX)		LO. Frequency（MHz）	Data HEX）
950——999	BA		1470——1529	A5
1000——1075	BC		1530——1649	A6
1076——1199	A0		1650——1799	A8
1200——1299	A1		1800——1949	AA
1300——1369	A2		1950——2150	AC
1370——1469	A4			

N8——N0： Programmable division ratio N control bits, N_{pro}:0—511。

$N_{pro}=N8\times2^8+N7\times2^7+\cdots+N2\times2^2+N1\times2^1+N0\times2^0$。

A4——A0： Programmable division ratio A control bits, A_{pro}:0—31。

$A_{pro}=A4\times2^4+A3\times2^3+A2\times2^2+A1\times2^1+A0\times2^0$。

NOTE: N and A Calculate：

A. LO. Frequency : 950MHz to 1075MHz：

$N_{pro}=f_{RF}$（MHz）÷8,

$A_{pro}=f_{RF}$（MHz）×2–N_{pro}×16；

B. LO. Frequency : 1076MHz to 2150MHz：

$N_{pro}=f_{RF}$（MHz）÷16,

$A_{pro}=f_{RF}$（MHz）–N_{pro}×16

G3——G0：IQ Gain Setting：

1110：+14 dB

0111：0dB

0010：-10dB

F4——F0：Base band filter setting bits：

$F_{pro}=F4\times2^4+F3\times2^3+F2\times2^2+F1\times2^1+F0\times2^0$。

NOTE:

A：If symbol rate(Sb) less than 30MHz，F_{pro} =Sb(MHz)；

B：If symbol rate(Sb) is 30MHz to 45MHz，F_{pro} =30。

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[4] CONFIGURATION REGISTERS

STV0288's Test Register Value Table：Write address: D0(HEX), Read address: D1(HEX)

Address. (H)	Data(H) 27.5Msps	Data(H) 5Msps	Address. (H)	Data(H) 27.5Msps	Data(H) 5Msps	Address. (H)	Data(H) 27.5Msps	Data(H) 5Msps
00	n/a	n/a	30	00	00	64	n/a	n/a
01	15	15	31	1E	1E	65	n/a	n/a
02	20	20	32	14	14	66	n/a	n/a
03	8E	8E	33	0F	0F	67	n/a	n/a
04	8E	8E	34	09	09	68	n/a	n/a
05	12	12	35	0C	0C	69	n/a	n/a
06	00	00	36	05	05	6A	n/a	n/a
07	n/a	n/a	37	2F	2F	6B	n/a	n/a
08	n/a	n/a	38	16	16	6C	00	00
09	00	00	39	BD	BD	70	00	00
0A	04	04	3A	00	00	71	00	00
0B	00	00	3B	13	13	72	00	00
0C	00	00	3C	11	11	74	00	00
0D	00	00	3D	30	30	75	00	00
0E	D4	D4	3E	n/a	n/a	76	00	00
0F	30	30	3F	n/a	n/a	81	00	00
10	n/a	n/a	40	63	63	82	3F	3F
11	80	80	44	04	04	83	3F	3F
12	03	03	42	60	60	84	00	00
13	48	48	43	00	00	85	00	00
14	84	84	44	00	00	88	00	00
15	45	45	45	00	00	89	00	00
16	B7	B7	46	00	00	8A	00	00
17	9C	9C	47	00	00	8B	00	00
18	00	00	4A	00	00	8C	00	00
19	A6	A6	4B	n/a	n/a	90	00	00
1A	88	88	4C	n/a	n/a	91	00	00
1B	8F	8F	50	10	10	92	00	00
1C	F0	F0	51	36	36	93	00	00
1E	n/a	n/a	52	09	09	94	IC	IC
1F	n/a	n/a	53	94	94	97	00	00
20	0B	0B	54	62	62	A0	48	48
21	54	54	55	29	29	A1	00	00
22	00	00	56	64	64	B0	B8	B8
23	00	00	57	2B	2B	B1	3A	3A
24	n/a	n/a	58	54	54	B2	10	10
25	n/a	n/a	59	86	86	B3	82	82
26	n/a	n/a	5A	00	00	B4	80	80
27	n/a	n/a	5B	9B	9B	B5	82	82
28	46	0C	5C	08	08	B6	82	82
29	65	CC	5D	7F	7F	B7	82	82
2A	E0	B0	0E	00	00	B8	20	20
2B	FF	FF	0F	FF	FF	B9	00	00
2C	F7	F7	60	n/a	n/a	F0	00	00
2D	n/a	n/a	61	n/a	n/a	F1	00	00
2E	n/a	n/a	62	n/a	n/a	F2	C0	C0
2F	n/a	n/a	63	n/a	n/a			

<note> (1) The data field with "n/a" stands for "read only register". No need write, no malady with writing,
(2) Some register bit should be swiched "l"and"0", during the signal search.
(3)symbol_frequency: SFRH.M.L[addreaa28.29.2A] = symbol_frequency / $F_{M.CLK}$[100MHz] x 2^{20}
(4) $F_{M.CLK}$ f_{PLL} = fxtal x (PLL_DIV)/4 when PLL_SELRATIO = 1
f_{PLL} = fxtal x (PLL_DIV)/6 when PLL_SELRATIO =0
(fxtal = 4MHz, PLL_SELRATIO[address:41, bit2]

STV0288 I2C Chip Address Selection

Tuner Pin 7 Voltage	Write Address	Read Address
0(GND or Open)	D0hex	D1hex
1(+3.3V)	D2hex	D3hex

[5] Fast channel acquisition and blind search

Automatic symbol rate search, signal acquisition and signal tracking are built into the STx0288 using a simple state machine controlled by I²C commands. The state machine significantly reduces the software needed and also decreases the duration of the transponders acquisition.

5-1 Control

The fast channel acquisition is performed in two steps. First step 'coarse auto search' enables rough estimation of a QPSK carrier within a given RF bandwidth. Second step 'Autos can' enables automatic lock to the previous estimated QPSK carrier.

5-1-1 First step: coarse auto search

- Coarse carrier and symbol frequency search
- Find appropriate symbol and carrier frequency in about 15 ms after tuner programming
- Range 1 to 45 Msps
- Accuracy of the estimation:

-carrier offset: ~ 1% Fs

-symbol rate: ~ 5%

5-1-2 Second step: autoscan

- Automatic symbol frequency scanning in any range.
- Automatic stop when the chip is locked
- Needs 1 Msymb to scan even at low C/N (3.5 dB)

5-2 Results

- Simplified scanning software routine versus STx0288
- Full satellite scanning in some seconds
- Fast channel acquisition

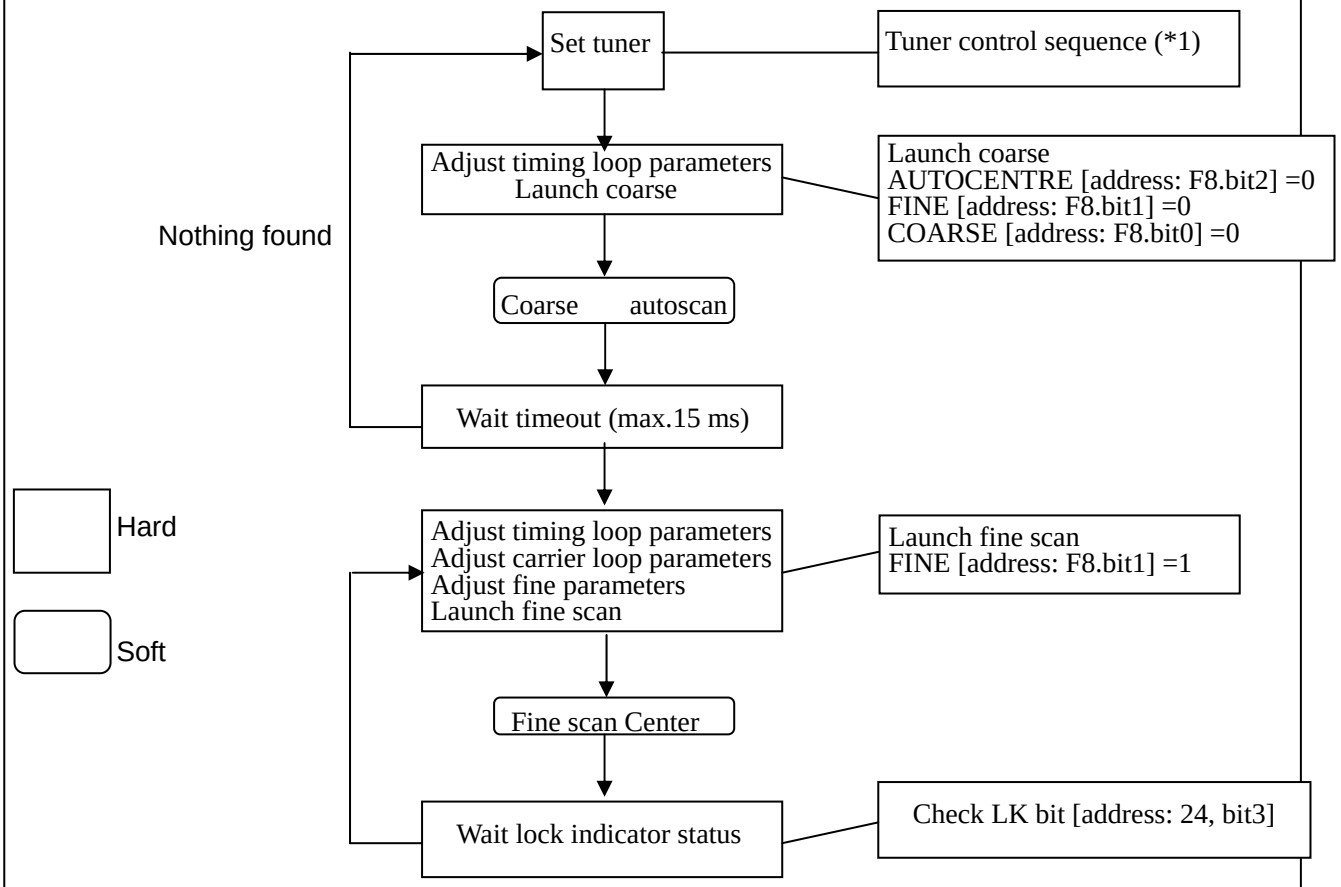
-Typical 15ms + 1 Msymbol duration

-Less than 120ms if fs > 10 MBd (channel unknown a priori)

-Around 5s around 2Msps (channel unknown a priori)

5-3. FLOW CHART

The following flow charts show recommended internal PLL and STB0288 control flows.



*1 Tuning details is down in the next section.

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[6] PLL Programming Sequence：

1、 Open I²C bus repeat；
2、 I²C bus start；
3、 Write address（C2h）；
4、 Write sub address（01h）；
5、 Write Reg01h to Reg0Bh data；
6、 I²C bus stop；
7、 Close I²C bus repeat；
8、 Open I²C bus repeat;
9、 I²C bus start；
10、 Write address（C2h）；
11、 Write sub address（07H）；
12、 Write data DFh;
13、 Write data D0h;
14、 Write data 50h;
15、 Write data FBh；
16、 I²C bus stop；

After tuner lock：

1、 Open I²C bus repeat；
2、 I²C bus start；
3、 Write address（C2h）；
4、 Write sub address（01h）；
5、 Write data (79h)；
6、 I²C bus stop；

NOTE:

Gain control: High input voltage corresponds to high gain

Please refer to the STB6000 and STV0288 datasheet for the programming

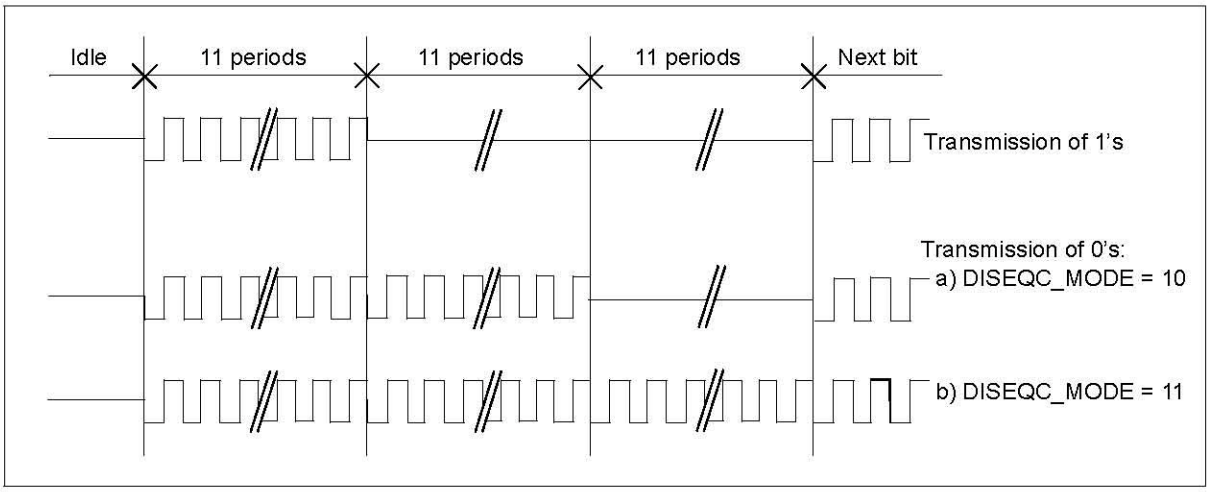
7 DiSEqC 2.x interface

7-1 Transmit DiSEqC interface

The transmit DiSEqC interface simplifies the real-time dialog between the microprocessor and the LNB. Using the I²C bus, the microprocessor fills an 8-byte FIFO, and then transmits the data by modulating the F22TX clock (F22TX is set to 22kHz beforehand).

7-1-1 Modulation.

Figure 2: Schematic showing bit transmission



The output is a gated 22 kHz square signal

- In idle state, modulation is permanently inactive.
- In byte transmission, the byte is sent (MSB first) and is followed by an odd parity bit.
  A byte transmission is therefore a serial 9-bit transmission with an odd number of 1's.
  Each bit lasts 33 F22 periods, and the transmission is PWM-modulated.

Transmission of 0's

There are two sub modes controlled by the I2C bus:

- modulation is active for 22 pulses, then inactive for 11 pulses (2/3PWM).
- modulation is active for 33 pulses (3/3 PWM).Transmission of 1's During transmission of 1's, modulation is active for 11 pulses, then inactive for 22 pulses (1/3 PWM).

This is compatible with tone burst in older LNB protocols.

For the modulated tone burst, only one byte (with value 0xFF) is written to the FIFO. The parity bit is 1. As a result, the output signal is nine 0.5 ms bursts, separated by eight 1-ms intervals.

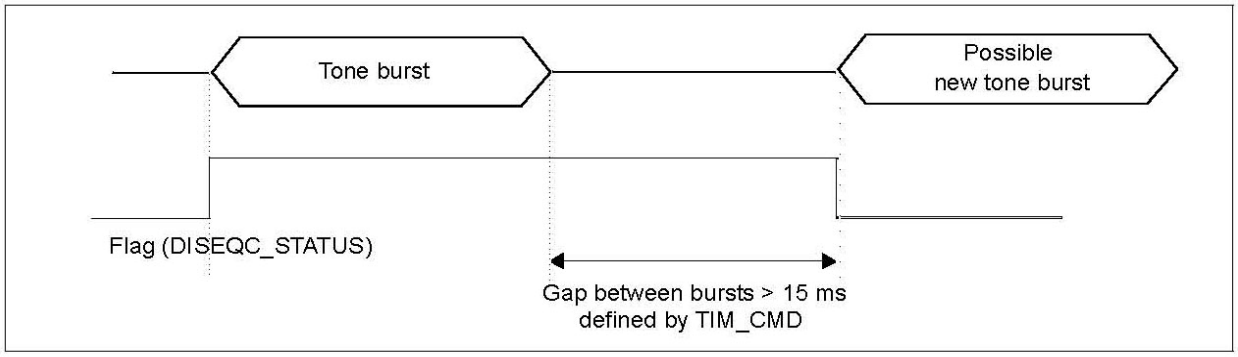
For the unmodulated tone burst, DISEQC_MODE = 11 and only one byte of value 0x00 is sent. The parity bit is still 1. As a result, the signal is a continuous series of 12.5 ms.

When the modulation is active, the DiSEqC output is forced alternatively to VDD and VSS levels.

7-1-2 Envelope mode

In envelope mode, a 22-kHz envelope output is generated instead of a modulated signal output. It controls the on/off switch of an external 22-kHz oscillator.

Figure 3: Gap between bursts



The backward compatibility of DiSEqC requires a 15-ms gap after a tone burst sequence. This information is delivered by a flag in a status register. This flag is set at the beginning of the transmission, and is reset after a time which includes both the transmission and a period defined by the I2C bus.

4.2 DiSEqC receive interface

The DiSEqC receive interface is composed of three parts, one analog and two digital.

- Analog: bypassable 1-bit analog-to-digital conversion,
- Digital filtering: envelop detection,
- Digital treatment: received byte extraction and stacking in FIFO, status management.

Figure 4: DiSEqC Rx analog part, running mode

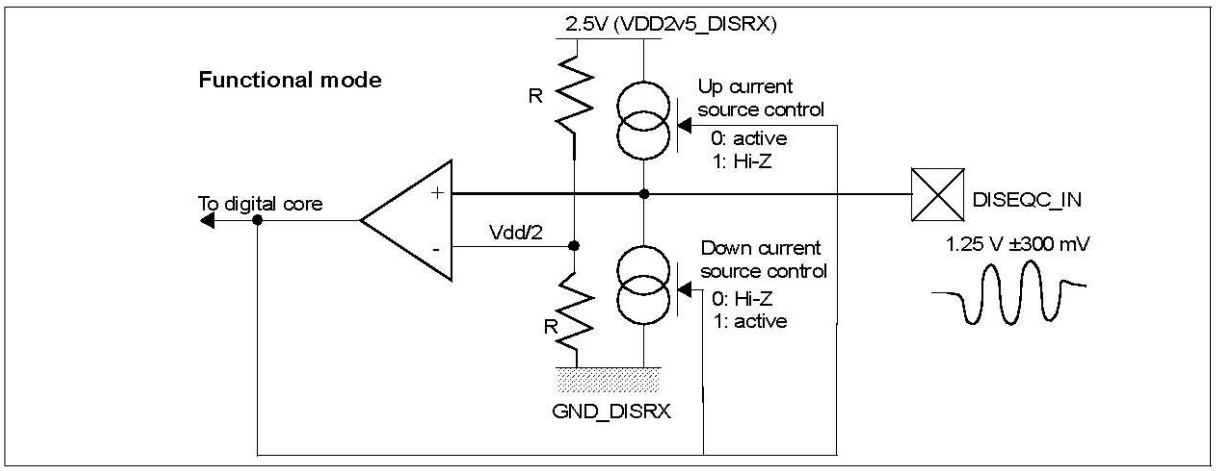
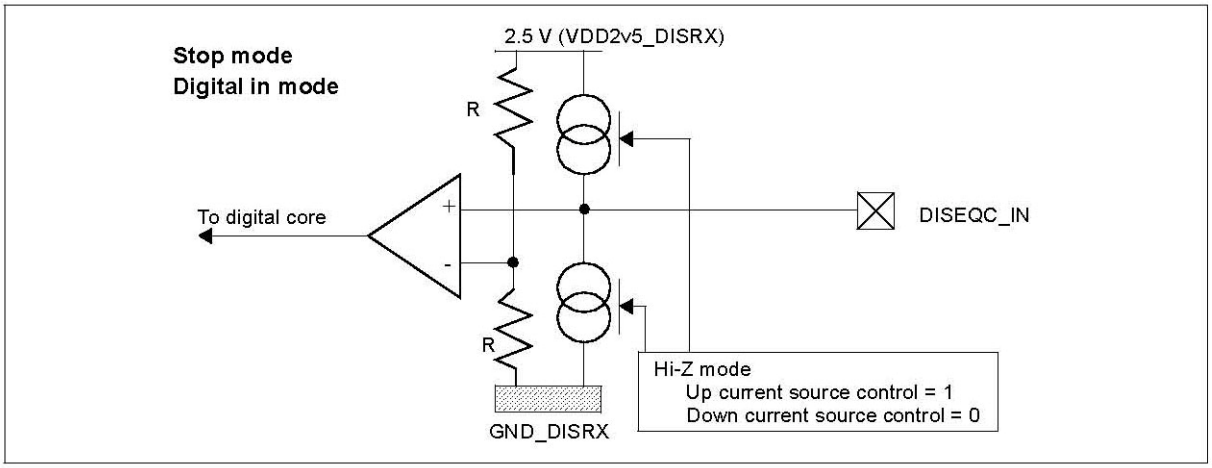


Figure 5: DiSEqC Rx analog part, stopped mode



General cell characteristics are as follows:

- 8-byte FIFO,
- bypass mode for analog cell:•the signal can be provided by a pin other than DISEQC_IN (or inverted DISEQC_IN),•IP0 or IP1 may be used, inverted or not,
- envelope mode: bypass of digital filtering,
- IRQ signals: fourth byte stacked in the FIFO and end of reception,
- 16-bit status register
- FIFO and parity output registers,•a non-null value in DISPARITY indicates a transmission error in the remaining data still stacked in the FIFO,
- other features:
  - ignore short 22-kHz mode: does not consider pulses composed of less than seven 22-kHz waves,• one-chip test mode: DISEqC Tx signal is injected in the DiSEqC Rx cell so the decoder understands the encoder,
  - continuous tone detection,•decoding fail detection and alert,
- 22-kHz frequency generation register: F22RX. The fully digital construction and independence of the analog cell enables the standard 22kHz to be increased up to 100kHz.

[8] Reliability

8-1. High temperature high humidity load (40℃, 90% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After cycling DUT in the constant chamber at 40℃/90-95% RH for 1.5h in on state and for 0.5h in off state, for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 9-1.

8-2. High temperature load (70℃, 40% RH, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant chamber at 70±2℃/40% RH for total 500h, leave the DUT at room temperature and humidity for 2h and then measure value after test.
3) Must meet the specifications of Table 9-1.

8-3. Cold test (-25℃, 500h)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial value.
2) After leaving DUT in the constant temperature chamber at -25℃ for 500h,leave the DUT at room temperature and humidity for 2h and then measure the values after test.
3) DUT must meet the specifications given in Table 9-1.

8-4. Shock (686 m/s2, 6 planes, 3 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the shock tester, apply shock of 686m/s2 three times to each of 6 planes and then measure the values.
3) DUT must meet the specifications given in Table 9-1.
4) This test is to be conducted using a single tuner.

8-5 Vibration (10-55 Hz, 1.5 mm, in each of three mutually perpendicular directions, each 2 times)

1) After leaving DUT at room temperature and humidity for 24h or longer, measure the initial values.
2) Using the vibration tester, apply motion having an amplitude of 1.5mm (constant), the frequency being varied uniformly between 10 and 55 Hz, to DUT, for 2 hours in each of three mutually perpendicular directions (X, Y and Z, total of 6 hours). After the test, measure the values.
3) DUT must meet the specifications given in Table 9-1.
4) This test is to be conducted using a single tuner.

8-6 Solderability of terminal Pretreatment of heating terminal at 150℃ for 1h is performed and leave it at room temperature for 2h or longer. Immerse 1.9 mm length of terminal (from the tip) to be soldered into rosin (JIS-K-5902), isopropyl alcohol (JIS-K-8839 or JIS-K-1522, rosin concentration (10-35% range) approx. 25% by weight unless otherwise specified) or equivalent solution for 3–5s, and then immerse the length of the terminal into a pool of molten solder (Sn/3.0Ag/0.5Cu, or equivalent) at 240±2℃ for 3s. Dipped terminal portion shall be wetted by more than 95%.

8-7 Soldering heat resistance immerse the terminal mounted on a PCB(1.6t thick) into solder at 350±5℃ for 3.0-3.5 seconds or at 260±5℃ for 10±1 seconds. Remove the PCB from the solder and leave it for 1 hour at room temperature. The test sample shall show no degradation in appearance and electrical characteristics.

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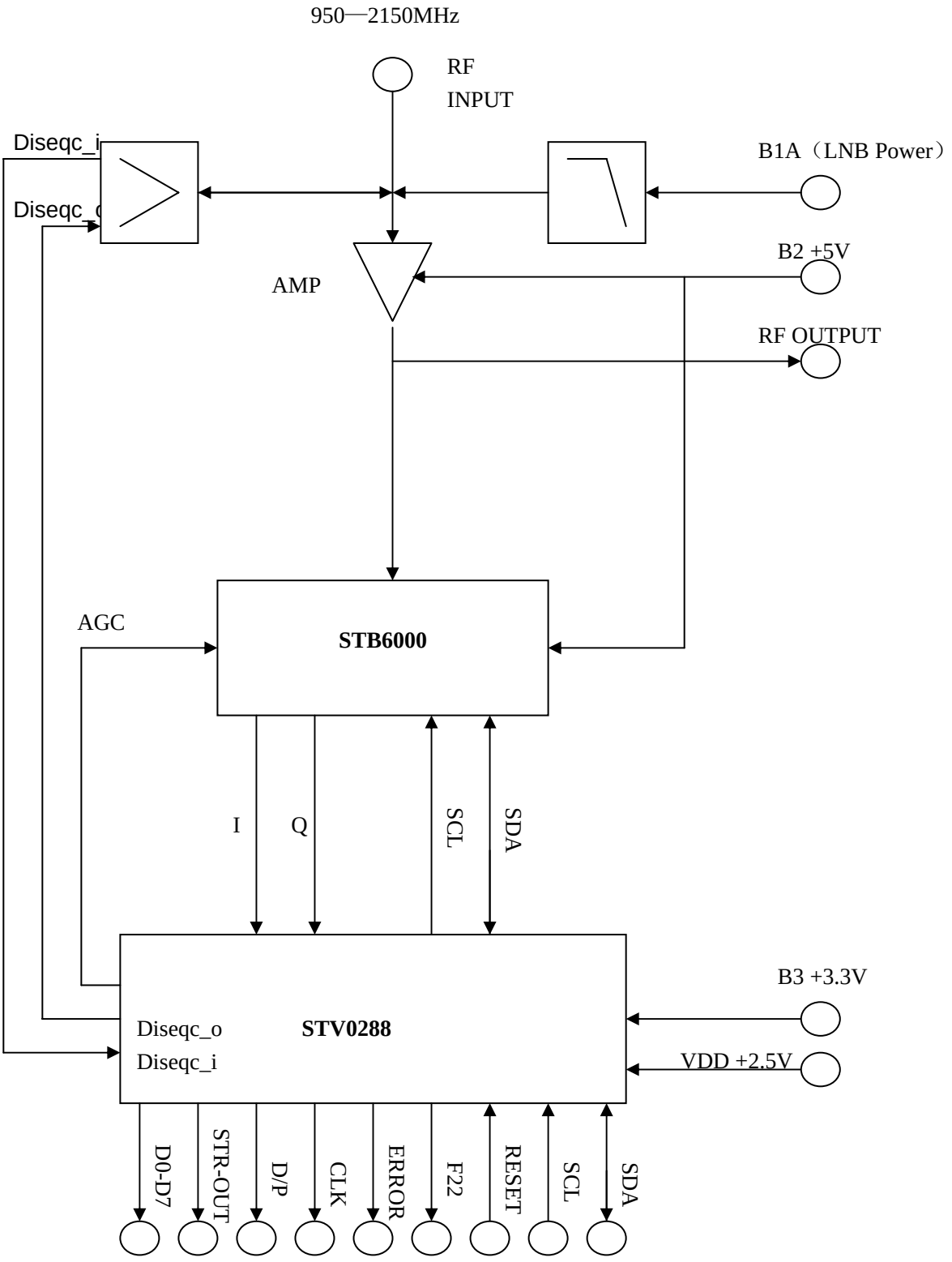
8-8 ESD protection

ESD test condition(IEC61000 4-2 compliant)

terminal	limits	Condition
RF_IN(coaxial center)	±15kV DC	150pf/300ohm each 5 times
Others	±200V DC	150pf/300ohm each 5 times

Item	Specification	Condition
Eb/No	(initial Values)±1db	BER=2e-4 at viterbi output PC=3/4

[9]System Block Diagram：



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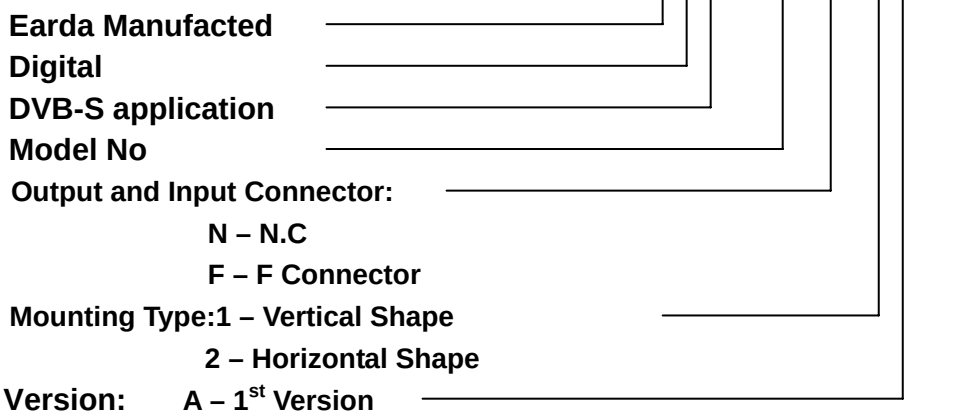
[10] Ordering Information

Model Name: E D S – 1547 F F 2 C



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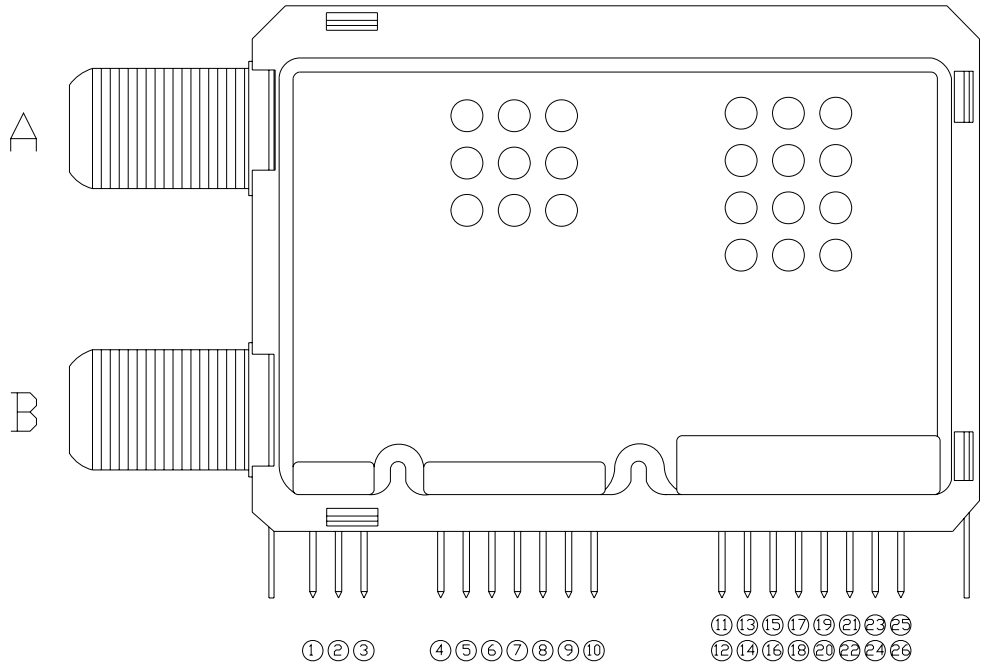
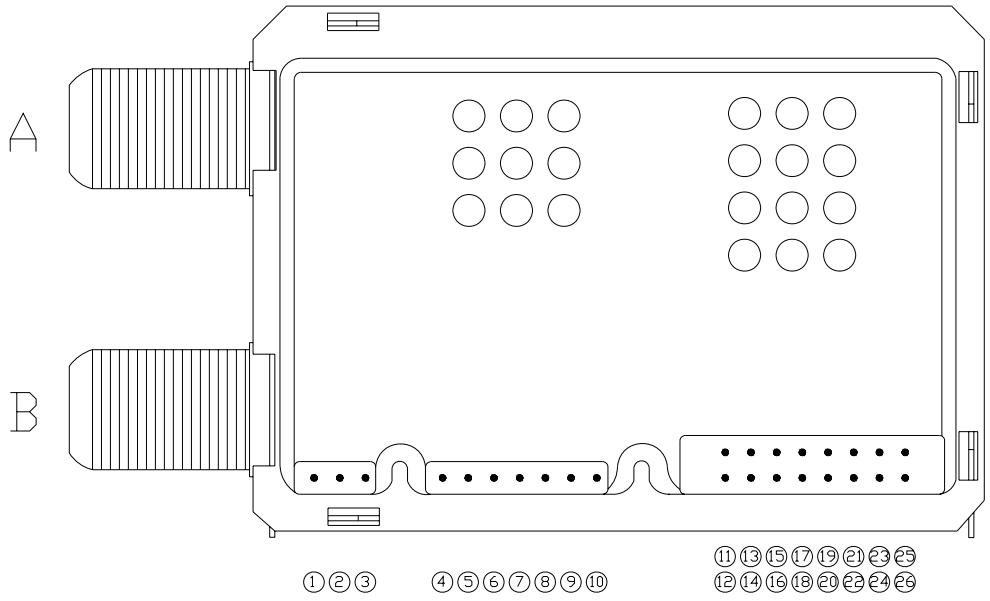
[11] Pin difinition

EDS-1547FF1C+



EDS-1547FF2C+ Pin Definition:



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Pin list：

PIN No.	PIN NAME	PIN DESCRIPTION
A	RF Input	950MHz——2150MHz Signal Input Terminal
B	RF Output	950MHz——2150MHz Signal Output Dispatch
1	B1B	RF output Voltage supply.
2	B1A	LNB Voltage supply.
3,4	NC	NC
5	B2	+5V Power Supply
6	NC	NC
7	AS	I2C Address Selection: 0(GND or Open) set to D0hex;1(+3.3V) set to D2hex
7	I2C Address	GND or Open: 0xd0; +3.3V: 0xd2
8	SDA	I^2C DATA Line
9	SCL	I^2C CLOCK Line
10	DISEQC IN	22K Pulse Signal Input For LNB
11	B3	+3.3V Power Supply
12	DISEQC OUT	22K Pulse Signal Output For LNB
13	VDD	+2.5V Power Supply
14，…，21	D0，…，D7	Transport stream output data，D7: Serial Output Data Bus
22	BCLK	Transport stream byte clock output.
23	D/P	Data Mark Output，1: Data Output, 0: Parity Output
24	STR OUT	Output〝1〞for the output of synchronization byte signal.
25	ERROR	Output〝1〞for the incorrect error occurred.
26	RESET	Reset. Please input 〝0〞for Reset.

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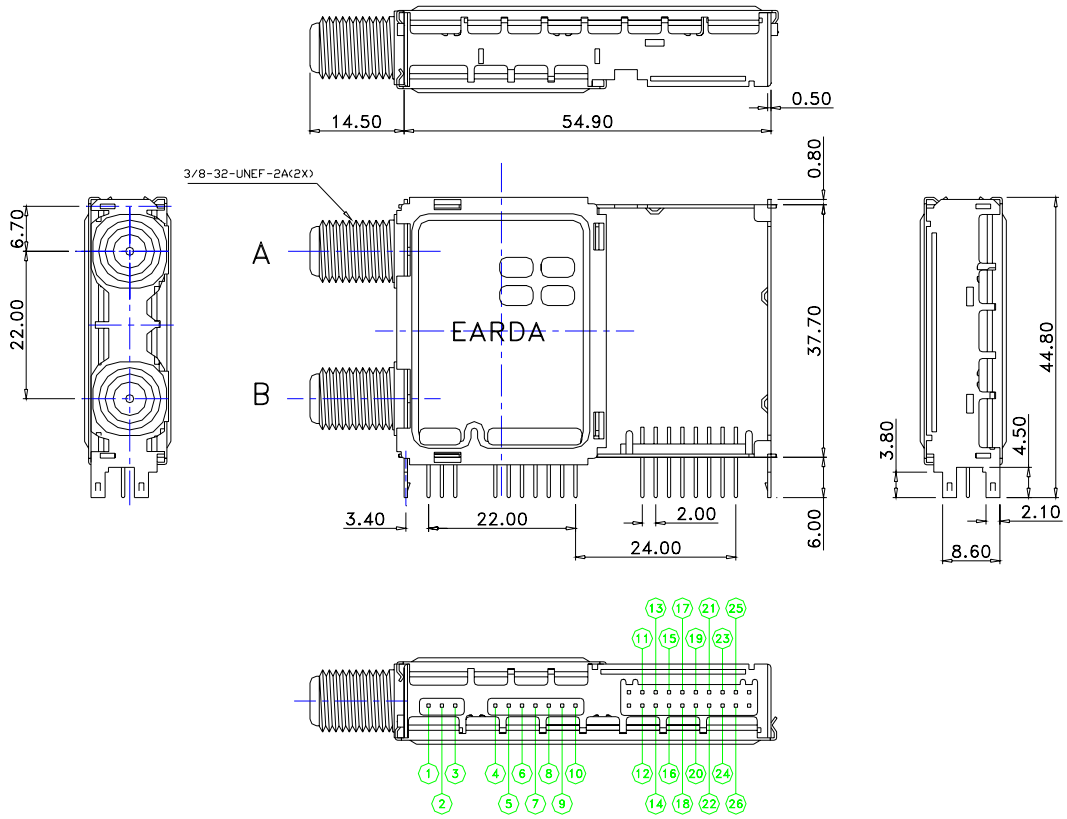
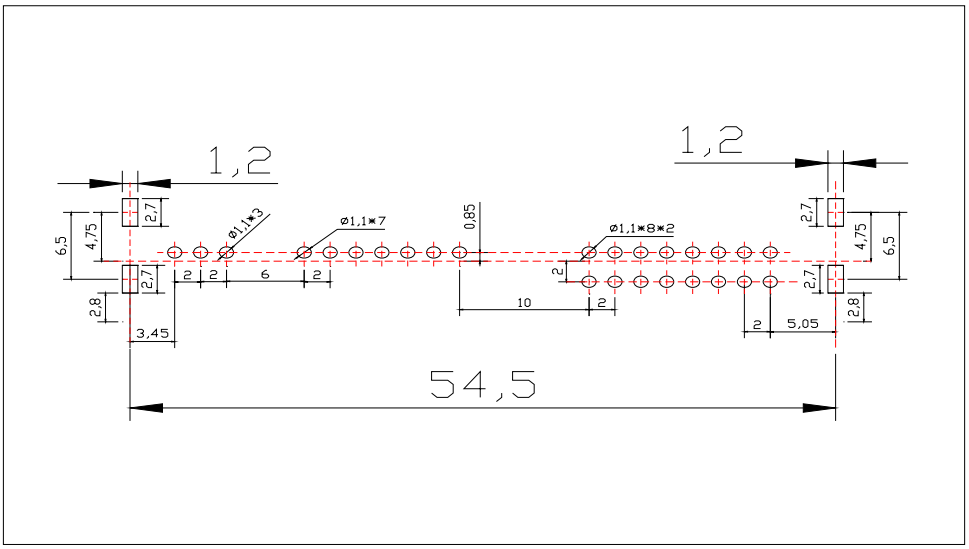
[12]Dimension for mounting：

EDS-1547FF1C+ Dimension

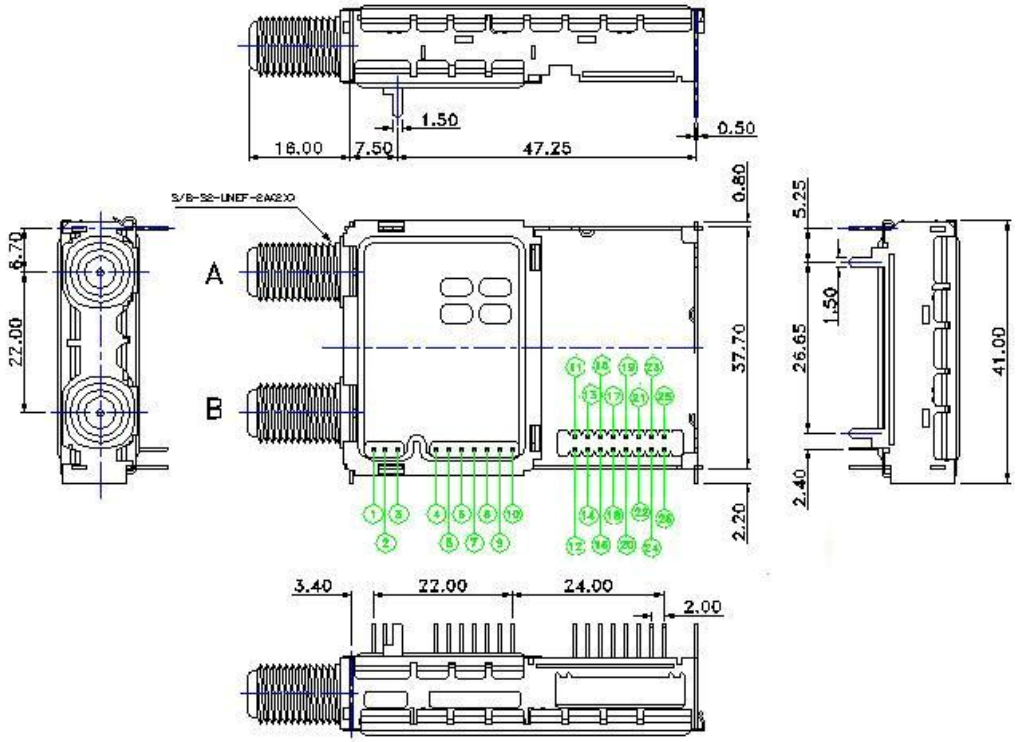


EDS-1547FF1C+ PCB Mounting



EARDA

EDS-1547FF2C+ Dimension



EDS-1547FF2C+ PCB Mounting